Dual VCO/PLL Synthesizer With IF Down-Conversion

FEATURES

- **Low Phase Noise**
- **High Dynamic Range Image-Reject Downconverter**
- **Selectable IF Filters**
- **Internal or External AGC Control With Peak Detector and Voltage Reference**
- **Analog Gain Control Range**
- **Direct Interface to A/D**
- **Dual VCO/PLL With On-Chip Resonator For Double Down-Conversion Architecture**

KEY SPECIFICATIONS

- **S-Band LO Frequency Range:**
  - **– TRF1112: 1700 to 2400 MHz**
  - **– TRF1212: 2400 MHz to 3550 MHz**
- **UHF LO Frequency Range: 325 MHz to 460 MHz**
- **Phase Noise is 0.5 RMS Typ 100 Hz to 1 MHz**
- **Rx Noise Figure of 5 dB, Typ**
- **UHF LO Tuning Step Size of 125 kHz With 18 MHz Reference**
- **Typical Gain of 90 dB, Including 15-dB Loss IF2 SAW Filter**
- **Input Third Order Intercept Point > 0 dBm**
- **Input 1-dB Compression Point > –10 dBm**
- **Gain Control Range of 90 dB Typ**

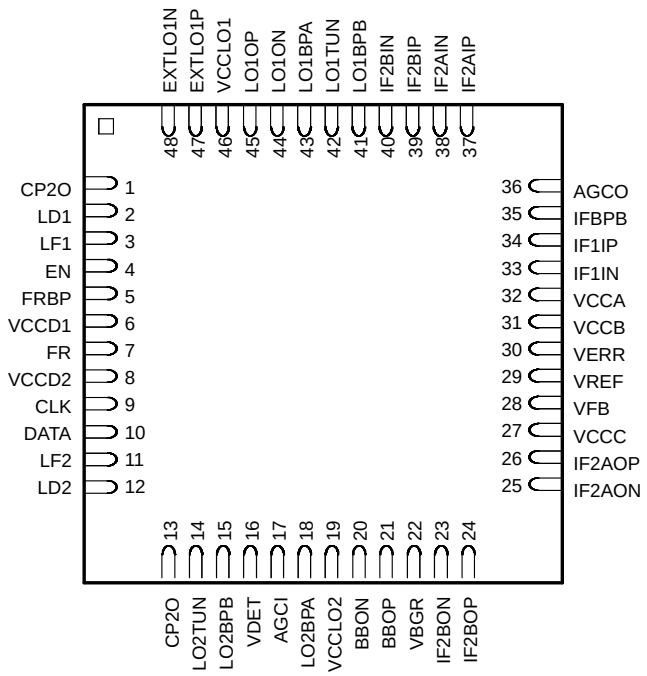
DESCRIPTION

The TRF1112 / TRF1212 are UHF-VHF down converters with integrated UHF and S-band frequency synthesizers for radio applications in the 2GHz to 4GHz range. The device integrates an image reject mixer, IF gain blocks, automatic gain control (AGC), and two complete phase locked loop (PLL) circuits including: VCOs, resonator circuit, varactors, dividers, and phase detectors.

The TRF1112 / TRF1212 are designed to function as part of Texas Instruments 2.5-GHz and 3.5-GHz complete radio chipsets, respectively. In the chipset, two chips function together to double-down convert RF frequencies to an IF frequency that is suitable for most baseband modem ADCs. The TRF1112 / TRF1212 performs the second down conversion from the first IF frequency (480 MHz typical) to a final IF frequency (20-50 MHz). The radio chipset features sufficient linearity, phase noise and dynamic range to work in single carrier or multi-carrier, line-of-sight or non-line-of-sight, IEEE standard 802.16, BWIF, or proprietary systems. Due to the modular nature of the chipset, it is ideal for use in systems that employ transmit or receive diversity.

TRF1112 / TRF1212 PIN OUT

LPCC−48 PACKAGE
(TOP VIEW)



BLOCK DIAGRAM

The detailed block diagram and the pin-out of the ASIC are shown in Figure 1 and the Terminal Functions table.

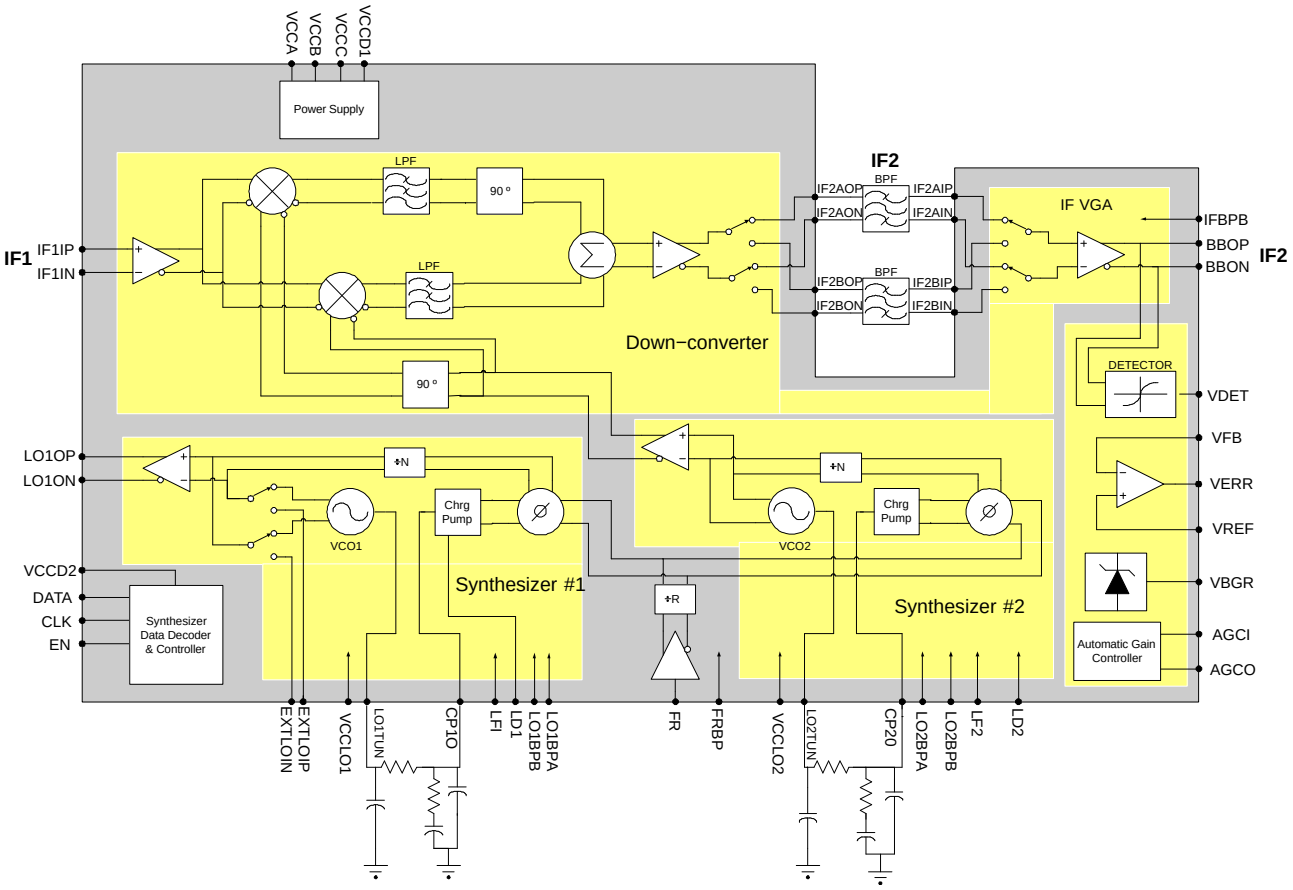


Figure 1. Detailed Block Diagram of TRF1112 / TRF1212

TERMINAL FUNCTIONS

TERMINAL		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	CP1O	O	Analog	Analog Synthesizer 1 Charge Pump Output
2	LD1	O	Digital	Synthesizer 1 Lock Detect Output, High is locked
3	LF1	O	Analog	Lock Detector Filter Capacitor for LO1, 0.01 µF Typ. 100 kΩ pull-up(1)
4	EN	I	Digital	3-wire bus Enable; Active High
5	FRBP	O	Analog	Reference Frequency Bypass, Internally biased to 2.5 V.
6	VCCD1	I	Power	Digital Power Supply Voltage
7	FR	I	Analog	Reference Frequency Source Input, HCMOS input. (DC level = 2.5 V)
8	VCCD2	I	Power	Digital Power Supply Voltage
9	CLK	I	Digital	3-wire bus Clock
10	DATA	I	Digital	3-wire bus Data
11	LF2	O	Analog	Lock Detector Filter Capacitor for LO2, 0.01 µF typ 100 kΩ pull-up(1)
12	LD2	O	Analog	Synthesizer 2 Lock Detect Output, High is locked
13	CP2O	O	Analog	Synthesizer 2 Charge Pump Output
14	LO2TUN	I	Analog	Synthesizer 2 VCO Input tune port
15	LO2BPB	O	Analog	Bypass cap for LO2, 0.1 µF (min) DCV = 1 V
16	VDET	O	Analog	Peak Detector Output

(1) Current leakage on the order of 10 µA through the capacitor or by any other means from either LF pin can cause false loss of lock signals. The two pull up resistors (R23 and R24) in Figure 20 reduce this sensitivity.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	TYPE	DESCRIPTION
NO.	NAME			
17	AGCI	I	Analog	AGC Voltage Input, 0-3 V
18	LO2BPA	O	Analog	Not connected for normal operation. DC bias nominal 1.8 V. Do not ground or connect to any other pin.
19	VCCLO2	I	Power	VCC for LO2, Low Noise Supply
20	BBON	O	Analog	IF output (differential) negative, DC coupled, internally biased to 3 V typical
21	BBOP	O	Analog	IF output (differential) positive, DC coupled, internally biased to 3 V typical
22	VBGR	O	Analog	Band-Gap Reference Voltage, 1.17 V
23	IF2BON	O	Analog	IF2B output (differential) negative, DC coupled, internally biased to 4 V typical
24	IF2BOP	O	Analog	IF2B output (differential) positive , DC coupled, internally biased to 4 V typical
25	IF2AON	O	Analog	IF2A output (differential) negative, DC coupled, internally biased to 4 V typical
26	IF2AOP	O	Analog	IF2A output (differential) positive, DC coupled, internally biased to 4 V typical
27	VCCC	I	Power	Analog Power Supply Voltage
28	VFB	I	Analog	Error Amplifier Feedback Input
29	VREF	I	Analog	Reference Frequency Input
30	VERR	O	Analog	Error Amplifier Output, internal op amp output
31	VCCB	I	Power	Analog Power Supply Voltage
32	VCCA	I	Power	Analog Power Supply Voltage
33	IF1IN	I	Analog	IF1 input (differential) negative, DC coupled, Internally biased to 1.4 V typical
34	IF1IP	I	Analog	IF1 input (differential) positive, DC coupled, Internally biased to 1.4 V typical
35	IFBPB	O	Analog	Bypass cap for IF amp, 0.1 μF (min), DCV = 1 V
36	AGCO	O	Analog	AGC Voltage Output Used to control Front end gain for extended dynamic range
37	IF2AIP	I	Analog	IF2A input (differential) positive, DC coupled, Internally biased to 3.0 V typical
38	IF2AIN	I	Analog	IF2A input (differential) negative, DC coupled, Internally biased to 3.0 V typical
39	IF2BIP	I	Analog	IF2B input (differential) positive, DC coupled, Internally biased to 3.0 V typical
40	IF2BIN	I	Analog	IF2B input (differential) negative, DC coupled, Internally biased to 3.0 V typical
41	LO1BPB	O	Analog	Bypass cap for LO1 0.1 μF (min), DCV = 1 V
42	LO1TUN	I	Analog	Synthesizer1 VCO Tune port Input
43	LO1BPA	O	Analog	Not connected for normal operation. DC bias nominal 1.8 V. Do not ground or connect to any other pin.
44	LO1ON	O	Analog	LO1 output (differential) neg. Negative and positive VCC bias (+5 V) for LO buffer amp.
45	LO1OP	O	Analog	LO1 output (differential) pos. Negative and positive VCC bias (+5 V) for LO buffer amp.
46	VCCLO1	I	Power	VCC for LO1, Low Noise Supply
47	EXTLO1P	I	Analog	External VCO input (differential) positive and logic level for VCO select.
48	EXTLO1N	I	Analog	External VCO input (differential) negative and logic level for VCO select.
–	BACK	–	–	Back side of package has metal base that must be grounded for thermal and RF performance.

ABSOLUTE MAXIMUM RATINGS

		UNIT
V_{CC}	DC Supply Voltage	0.0 V to 5.5 V
I_{CC}	DC Supply Current	270 mA
Pin	RF Input Power	20 dBm
T_J	Junction Temperature	150°C
Pd	Power Dissipation	1.5 W
	Digital Input Pins	–0.3 to 5.5 V
	Analog Input Pins	TBD
θ_{JC}	Thermal Resistance Junction-to-Ambient(1)	25°C/W
T_{stg}	Storage Temperature	– 40°C to 105°C
T_{op}	Operating Temperature	–40°C to 85°C
	Lead Temperature, 40 Sec Max.	260°C

(1) Thermal resistance is junction to ambient assuming thermal pad with 16 thermal vias under package metal base see recommended PCB layout (see Figure 20.)

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V, T = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage		4.8		5.2	V
I_{CC}	DC supply current			200		mA

DOWNCONVERTER ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C, FIF = 480 MHz, IF2 SAW 43.75 MHz unless otherwise stated

OVERALL DOWNCONVERTER SIGNAL CHARACTERISTICS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IF1}	IF1 input frequency		400	480	500	MHz
G_{max}	Maximum gain	IF1IP/N to BBOP/N at V_{AGC}I = 3 V	90	95	100	dB
DR_G	Gain control range	IF1IP/N to BBOP/N at V_{AGCI} = 0 through 3 V	78	90		dB
ΔG_{max}	Gain flatness	IF1IP/N to IF2A/BOP/N or BBOP/N for any gain setting. Measured in 6 MHz BW, excluding BPF gain variations		±0.3		dB
IR	Image rejection	IF1IP/N to IF2A/BOP/N Measured into 1 kΩ differential load IF2 = 35–60 MHz	30	35		dBc
NF	Noise figure	High Gain (V_{AGCI} = 2 V) IF1IP/N to BBOP/N at 100 Ω diff		4.7		dB
IP-1dB	Input power at 1dB gain compression	High Gain (V_{AGCI} = 2 V) IF1IP/N to BBOP/N at 100 Ω diff		–75		dBm
		Low Gain (V_{AGCI} = 0 V) IF1IP/N to BBOP/N at 100 Ω diff		–10		
IIP3	Input 3rd order intercept	High Gain (V_{AGCI} = 2 V) IF1IP/N to BBOP/N at 100 Ω diff		–65		dBm
		Low Gain (V_{AGCI} = 0 V) IF1IP/N to BBOP/N at 100 Ω diff	–5	0		
Z_{IF1}	IF1 input impedance	Differential mode		100		Ω
RL_{IF1}	IF1 input return loss	Measured into 100 Ω differential load at IF1P/N input	–11	–16		dB
f_{IF2}	IF2 frequency		25		70	MHz
Z_{IF2O}	IF2A/BO output impedance	Measured in differential mode At IF2A/BOP/N		50		Ω
ISO_{PP}	Port-to-port isolation	Measured between IF2AOP/N to IF2BOP/N and IF2AIP/N to IF2BIP/N with the Filter Select set high or low.	30			dB
ISO_{OI}	Output-to-input port isolation	Measured between IF2A/BOP/N and IF2A/BIP/N with the Filter Select set high or low.	60			dB
Z_{F2I}	IF2A/BI input impedance		1	2		kΩ
$V_{BB,OUT}$	Output signal level	Measured into a 1000 Ω differential load at BBOP/N at any gain with functional AGC	1.2			Vppd
IMD	In-band intermodulation	Closed-loop AGC, $V_{BB,OUT}$ = 1.2 V Any input power up to –20 dBm.		–35	–30	dBc

DOWNCONVERTER ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 5 V, T_A = 25°C, FIF = 480 MHz, IF2 SAW 43.75 MHz unless otherwise stated

OVERALL DOWNCONVERTER SIGNAL CHARACTERISTICS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{BB}	Baseband section output impedance	Measured in differential mode at BBOP/N		50		Ω

SYNTHESIZER #1 (S-BAND PLL) ELECTRICAL CHARACTERISTICS

SYNTHESIZER #1 SIGNAL CHARACTERISTICS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{Ref}	Reference frequency	Reference frequency can vary. 18 MHz is used for reference design Also see 1 Note that for source peak-to-peak voltages of less than 4 V and dc component other than 2.5-V degradation of the close-in phase noise may occur. For oscillators with no dc component, a dc voltage may be applied using a voltage divider (see the schematic and the Input Reference Requirements table).		18		MHz
f_{LO1}	Output frequency range	TRF1112	1700		2400	MHz
		TRF1212	2400		3550	
MS_{LO1}	Tuning sensitivity	TRF1112, For V_{LO1TUN}≥ 2 V	200		400	MHz/V
		TRF1212, For V_{LO1TUN}≥ 2 V	300		600	
Δf_{LO1}	Step size, nominal	For 18-MHz reference input		1		MHz
P_{LO1}	Power level	Measured into a 100-Ω differential load at the LO1OP/N port, over temperature and frequency range	-6	-3	0	dBm
$\phi_{FR\ VOC1}$	Free running VCO1 SSB phase noise at 100 kHz	Measured into 100-Ω differential load at the LO1OP/N port		–100		dBc/Hz
$\phi_{LD\ LO1}$	Locked synthesizer 1 SSB phase noise at 10 kHz	Measured into 100-Ω differential load at the LO1OP/N port Locked with loop bandwidth set to 400 kHz nominal		–105		dBc/Hz
	Locked Synthesizer 1 SSB phase noise at 100 kHz			–100		
$\phi_{LD\ LO1}$	Locked Synthesizer 1 Integrated RMS phase noise	100 Hz to 1 MHz		0.5	1	deg
$R_{RS\ LO1}$	Reference Spur Rejection	Measured into a 100-Ω differential load at the LO1OP/N port			–50	dBc
$R_{FS\ LO1}$	Fractional Spur Rejection	Measured into a 100-Ω differential load at the LO1OP/N port			–45	dBc
$R_{N\ x\ LO1}$, N: 2,3,4…	Harmonic Rejection	Measured into a 100-Ω differential load at the LO1OP/N port		–20		dBc
RL_O	Output Return Loss	Measured into a 100-Ω differential load at the LO1OP/N port over all input power levels.	–11	–16		dB
Z_O	Output Impedance	Differential mode at LO1OP/N port		100		Ω
P_{extVCO}	Ext VCO input	Differential mode		–13		dBm
$R_{LextVCO}$	Ext VCO Port Input Return Loss	Differential mode		–13		dB
$Z_{I\ extVCO}$	Ext VCO port input impedance	Differential mode		100		Ω

SYNTHESIZER #2 (UHF-BAND PLL) ELECTRICAL CHARACTERISTICS

SYNTHESIZER #2 SIGNAL CHARACTERISTICS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{Ref}	Reference Frequency	See Table 4		18		MHz
f_{LO2}	Frequency		325		460	MHz
$\phi_{FR\ VCO2}$	Free running VCO2 SSB Phase Noise at 100 kHz			–115		dBc/Hz
$\phi_{LD\ LO2}$	Locked Synthesizer 2 SSB Phase Noise at 10 kHz			–115		dBc/Hz
$\phi_{LD\ LO2}$	Locked Synthesizer 2 SSB Phase Noise at100 kHz			–115		dBc/Hz

SYNTHESIZER #2 (UHF-BAND PLL) ELECTRICAL CHARACTERISTICS (continued)

SYNTHESIZER #2 SIGNAL CHARACTERISTICS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\phi_{LD\ LO2}$	Locked Synthesizer 2 Integrated RMS Phase noise	100 Hz to 1MHz			0.2	deg
MS_{LO2}	Tuning Sensitivity	For $V_{LO2TUN} \geq 2$ V	40		80	MHz/V
Δf_{LO2}	Step Size	For 18-MHz reference input			125	kHz
$R_{RS\ LO1}$	Reference Sideband Rejection			–65	-60	dBc
$R_{FS\ LO1}$	Fractional Spurs Rejection			–65	–60	dBc

INPUT REFERENCE REQUIREMENTS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{Ref}	Reference Frequency			18		MHz
	Temperature Stability	Customer Requirement				
V_{FR}	Reference Source Input Level(1)	HCMOS Output	4	4.5	5	Vpp
	Reference Input Symmetry	Waveform Duty Cycle	40%		60%	
τ_{FR}	Waveform Pulse Rise Time	10% to 90% of max voltage transition		1	4	nsec
ϕ_{FR}	SSB Phase Noise at 10 kHz			–153	–150	dBc/Hz

(1) Note that for source peak-to-peak voltage of less than 4 V and dc component other than 2.5-V degradation of the close-in phase noise may occur. For oscillators with no dc component, a dc voltage may be applied using a voltage divider (see the schematic).

AC TIMING, SERIAL BUS INTERFACE

SERIAL INTERFACE TIMING CHARACTERISTICS (see Figure 9)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{DI}	Clock to Data Invalid		10			ns
D_VC	Data Valid to Clock		10			ns
C_{PWH}	Clock Pulse Width High		50			ns
C_{PWL}	Clock Pulse Width Low		50			ns
CE_L	Clock to Enable Low		10			ns
E_LC	Enable Low to Clock		10			ns
E_{PWH}	Enable Pulse Width		10			ns

DIGITAL INTERFACE CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage		2.1		5.0	V
V_{IL}	Input Low Voltage		0		0.8	V
I_{IH}	Input High Current		0		50	µA
I_{IL}	Input Low Current		0		–50	µA
C_I	Input Capacitance			3		pF
V_{OH}	Output Logic 1 Voltage	0 to 100-µA load	2.4		3.6	V
R_{OH}	Output Logic 1 Impedance			18		kΩ
V_{OL}	Output Low Voltage	0 to -100-µA load	0		0.4	V

AUXILIARY, AGC, AND CONTROL FUNCTIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VCOenbl}$	External VCO Enable Voltage	CMOS compatible Input. See the Synthesizer #1 (S-Band PLL) Characteristics table.				V
V_{LD1}	Lock Detect Voltage (PLL1)	CMOS compatible Output (active high). See the Synthesizer #1 (S-Band PLL) Characteristics table.				V
V_{LD2}	Lock Detect Voltage (PLL2)	CMOS compatible Output (active high). See the Synthesizer #1 (S-Band PLL) Characteristics table.				V
V_{AGCI}	Gain Control Input		0		3	V
V_{AGCO}	Gain Control Output	When loaded with 10-kΩ load. Output impedance of AGCO is 3.75 kΩ. Texas Instruments RF ASICs present a 10-kΩ load impedance.	0		1.5	V
A_{AGC2}	VAGCO Accuracy	V_{AGCO} vs V_{AGCI} characteristic	±100			mV
V_{DET}	Detector Output Voltage		TBD			mV
A_{VDET}	Detector Accuracy		TBD			mV
V_{BGR}	Band-Gap Reference Voltage		1.17			V
t_{RBB}	AGC Time Constant	Set by external loop filter	TBD			µs
EXTLOIP	On-chip VCO1 selection	Logic level applied to EXTLOIP and EXTLOIN pins to select the on-chip VCO		High		
EXTLOIN				High		
EXTLOIP	Off-chip VCO1 selection	Logic Level applied to EXTLOIP and EXTLOIN pins to select the off-chip (external) VCO.		Low		
EXTLOIN				Low		

The V_{AGCO} vs V_{AGCI} is the voltage-transfer-function as defined by Table 1 when the AGCO is loaded with 10 kΩ. Note: The RFAGC pin on Texas Instruments RF downconverters (such as: TRF1111, TRF1115, or TRF1216) have an internal load of 10 kΩ and consequently the user should not add a separate 10-kΩ load resistor.

Table 1. AGCO Voltage vs AGCI Voltage

VAGCI	V	0.0	0.1	0.2	0.3	0.4	0.5	0.6	>0.6
VAGCO	V	1.5	1.2	0.85	0.55	0.2	0.0	0.0	0.0

FREQUENCY PLAN

The TRF1112 / TRF1212 allow a variety of frequency plans. Figure 2 illustrates the allowable combinations of first and second IFs. However, due to the fact that the chips feature image-reject mixers, significant changes in the frequency plan can result in degradation of image rejection. This phenomenon is captured in Figure 3.

In order to maintain maximum image rejection and LO suppression, a recommended frequency plan is: RxIF1 = 480 MHz, RxIF2 = 43.75 MHz.

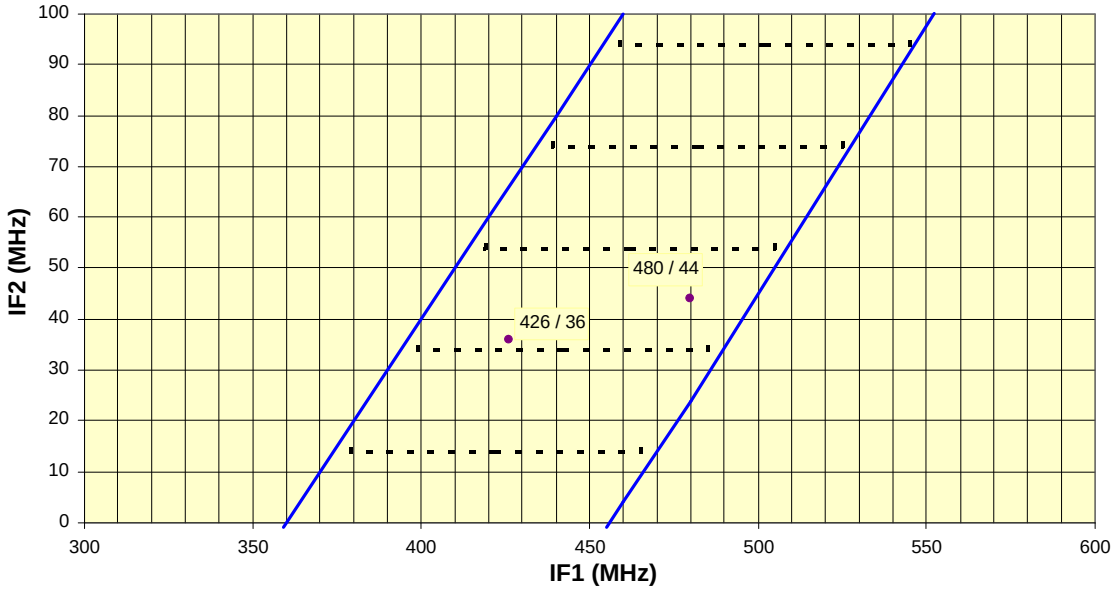


Figure 2. Potential Receive IF Combinations

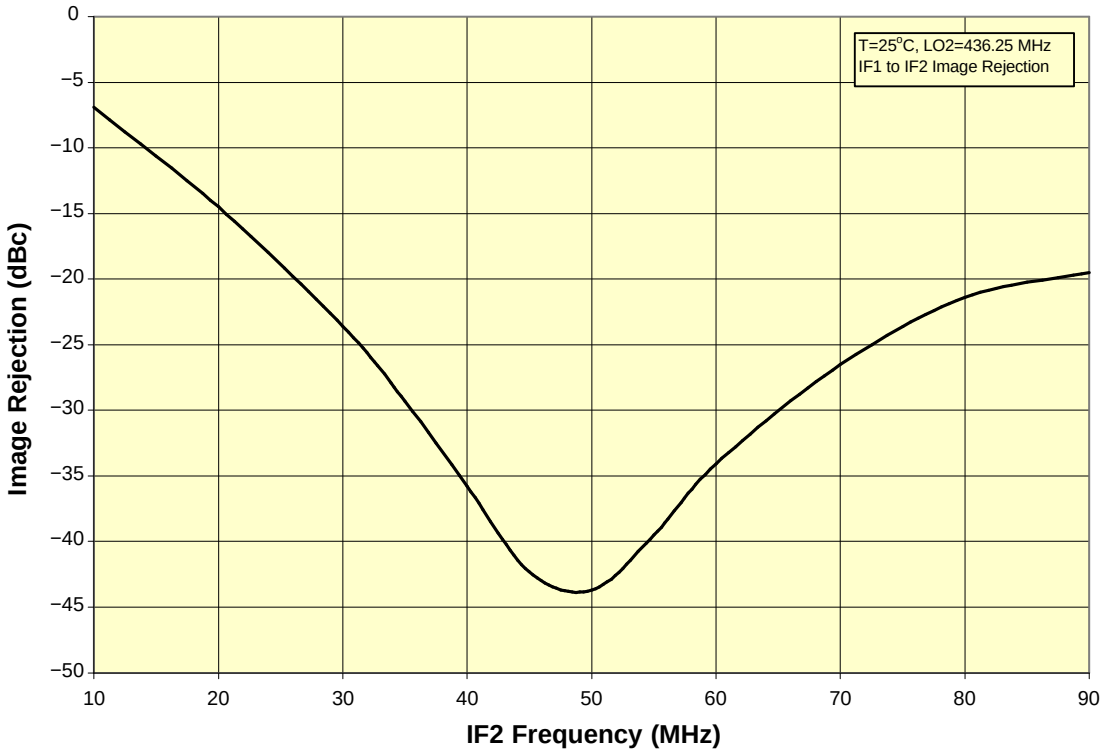


Figure 3. Image Rejection vs IF2

RECEIVE GAIN CONTROL

The TRF1112 / TRF1212 offers two methods for gain control. Gain can be adjusted via an external analog signal (0-3 V) or by using the on-chip detector, voltage reference and operational amplifier.

The gain-response curve is shown in Figure 4 and is designed to be monotonic for a 0-V to 3-V input analog voltage. This voltage control (AGCI) can be used to keep a constant peak-to-peak differential voltage output from

the TRF1112 / TRF1212 to the baseband processor's ADC over a large input signal dynamic range. The recommended TRF1112 / TRF1212 differential output level is 1.2 Vpp. The ASIC AGC output pin (AGCO) can be used to control the gain of a front-end downconverter for improved system dynamic range. In order to minimize the receiver's noise figure, the gain is changed in a stepped fashion. This means as the input signal level decreases, the gain shifts from the front-end stages to the back-end stages of the chip. This approach allows the noise figure to remain low until large input signals are present.

Closed-Loop AGC

In order to achieve very fast signal acquisition in applications such as burst-mode transmission, Texas Instruments offers a receive gain control loop that requires no interaction from the demodulator. The internal loop operates by comparing the output of an internal peak detector to an internal voltage reference and adjusting the gain of the receive chain such that a constant voltage is achieved over a large input signal dynamic range. The internal AGC speed is set by an external AGC loop filter, the speed of which should be set low enough so that the AGC loop will not remove any carrier AM modulation.

Careful attention to the ASIC architecture enables excellent 3rd order intermodulation distortion (IMD) performance over the entire AGC range as shown in Figure 4 and Figure 5. In these figures, VREF refers to the reference voltage setting on the VREF pin which is used to set the output voltage swing when configured for internal AGC. Vout is the output voltage swing at IF2 given in Vpp differential or rms.

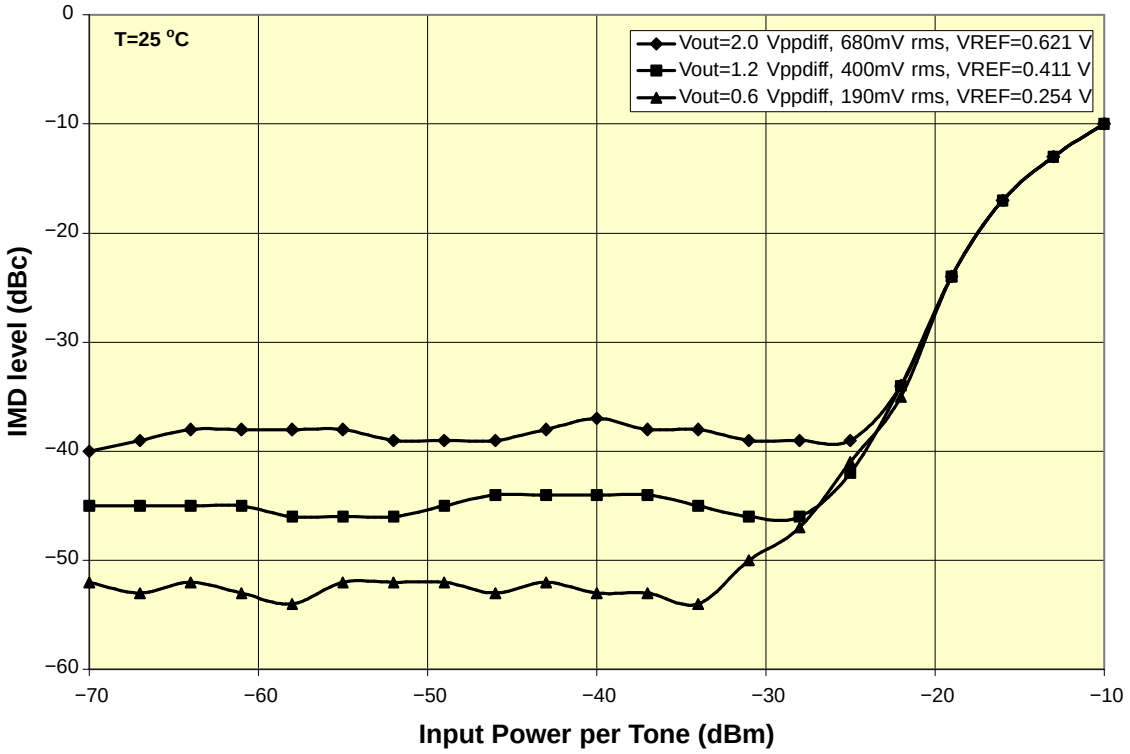


Figure 4. IMD Level vs Input Power and AGC Output Setting (IF2 BPF Loss of 15 dB Included in Plot)

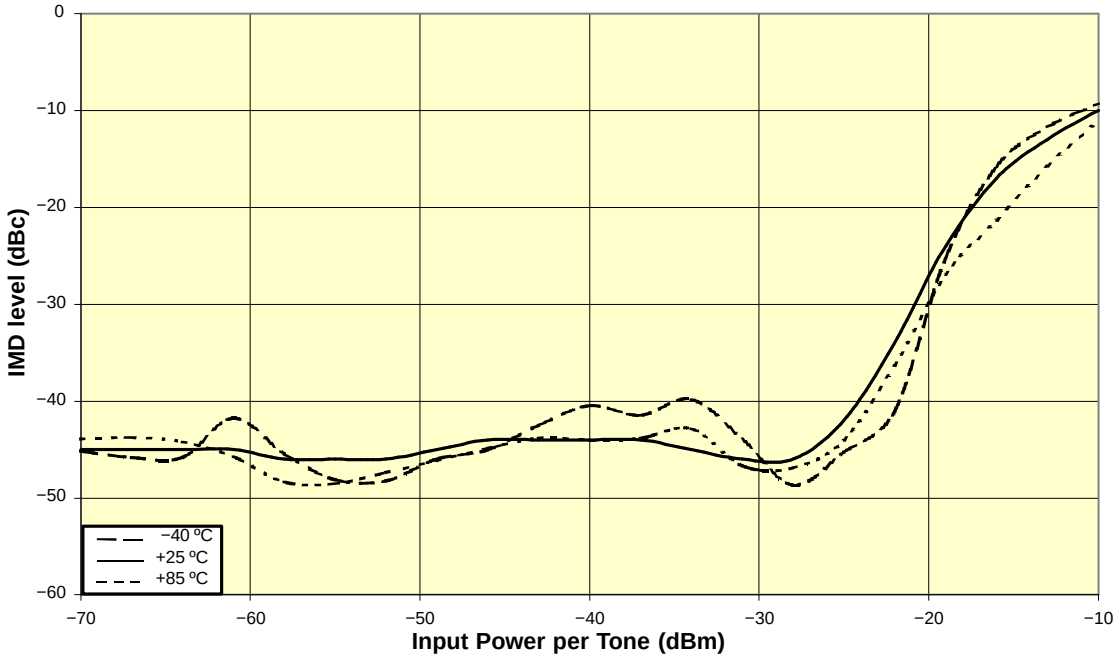


Figure 5. IMD Level vs Temperature at Output AGC Setting of 1.2-Vpp Differential (IF2 Filter Loss of 15 dB Included)

External Analog Control

Receive signal gain control can also be accomplished through direct interaction with the modem. For example, the modem can look at several metrics on the incoming signal including voltage swing, SNR, and AGC error, then feedback an analog (0 V to 3 V) gain control signal to the Texas Instruments ASIC. Note that for applications requiring large channel bandwidths (e.g., 6 MHz) the maximum usable VAGCI should be limited to approximately 2 V to 2.5 V, otherwise the resulting gain produces excessive amounts of noise at the output.

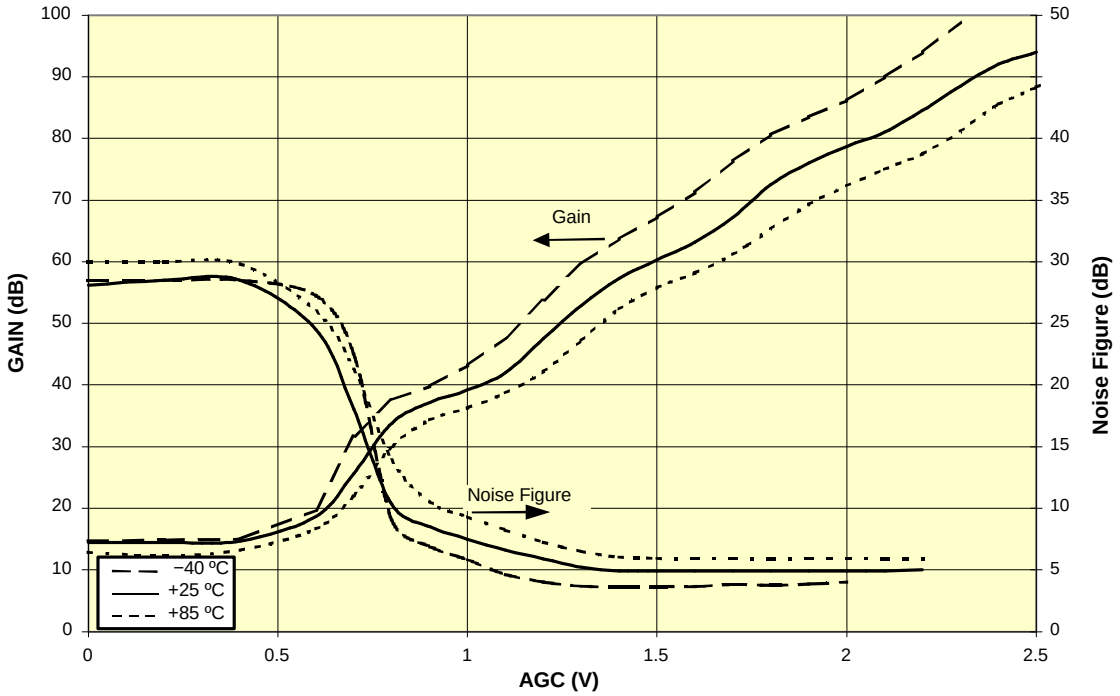


Figure 6. TRF1112 / TRF1212 Gain vs AGCI Voltage (IF2 BPF Loss of 15 dB Included)

Figure 7 shows the input third-order intercept point (IIP3) vs V_{AGCI} for open loop AGC operation. As expected, the IIP3 decreases with increasing gain (increasing V_{AGCI}). The input P-1dB behaves in a similar way.

Figure 8 shows that the output P-1dB (OP-1dB) and output (OIP3) of the TRF1112 / TRF1212 is approximately constant vs the V_{AGCI} voltage.

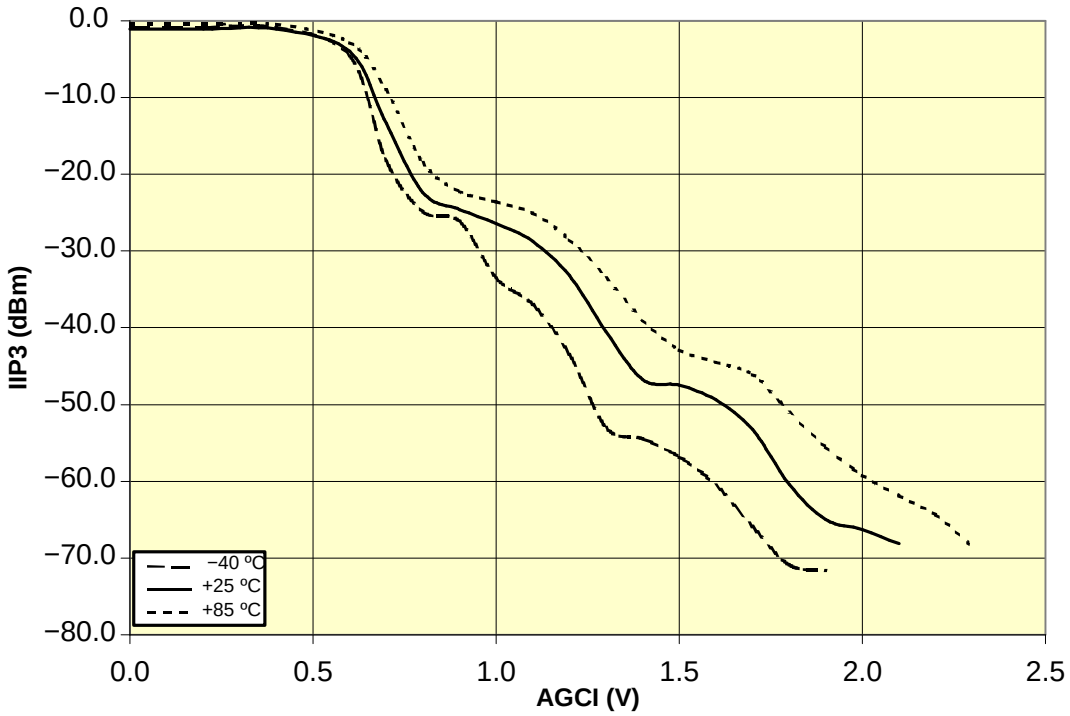


Figure 7. IIP3 vs AGCI Voltage and Temperature (IF2 BPF Loss of 15 dB Included)

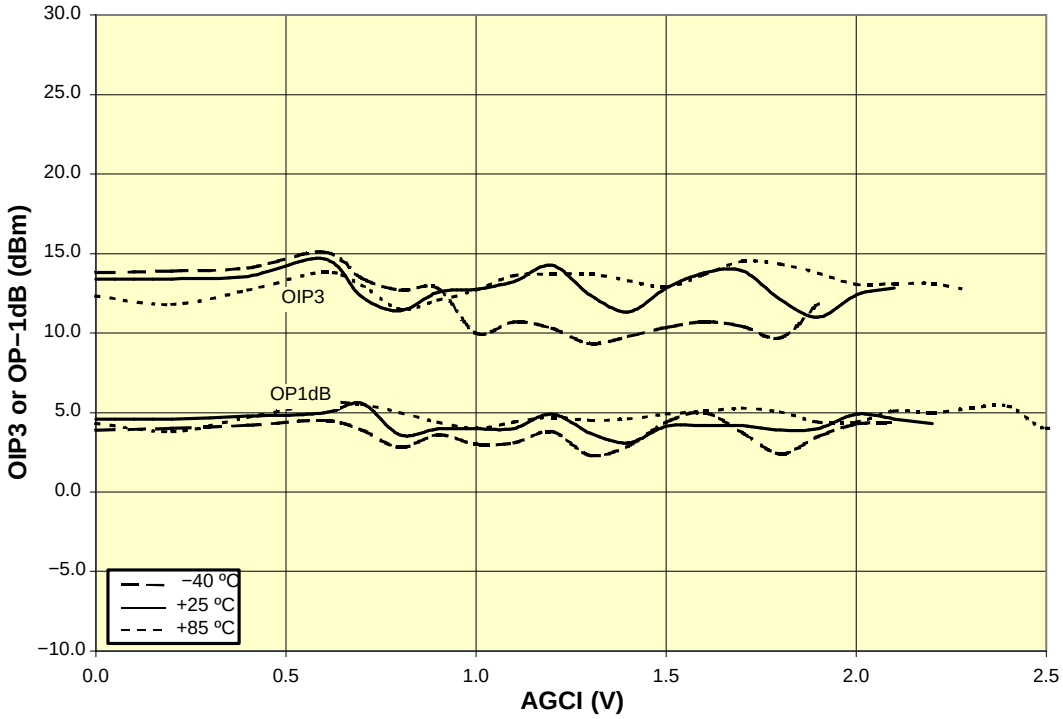
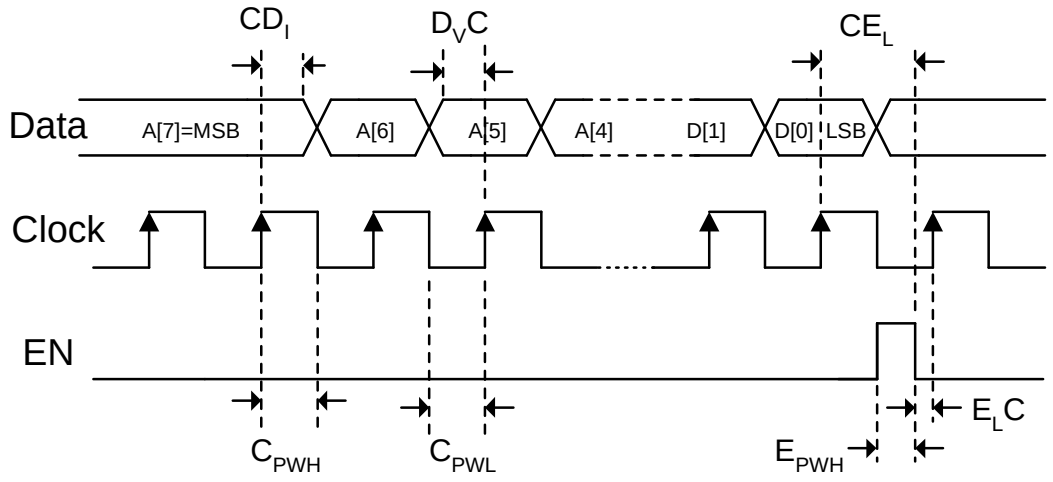


Figure 8. OP-1dB and OIP3 vs AGCI Voltage and Temperature (IF2 BPF Loss of 15 dB Included)

INTEGRATED SYNTHESIZERS

PLL Programming

A UHF and S-band PLL are integrated in the TRF1112 / TRF1212. These two PLLs can be programmed via a 3-wire serial bus (CLK, DATA, and EN) from the baseband processor. The timing specs are given in the AC Timing table and detailed in Figure 9. Figure 10details the addresses and register values required to fully program the synthesizers.



NOTE: If left unconnected, the DATA, CLK and EN pins rest on logic *High*.

Figure 9. Serial Interface Timing Diagram

Data is written to the PLLs according to the following format:

MSB							Byte 1	LSB	MSB					Byte 2			LSB	MSB					Byte 3			LSB
Address									Data																
A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]		D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0	0	0	0	0	0	0	0		0	0	Synth #1 N divider							Synth #1 S counter			Synth #1 F divider				
0	0	0	0	0	0	0	1		0	0	Synth #2 N divider							Synth #2 S counter			Synth #2 F divider				
0	0	0	0	0	1	0	0		0	0	0	0	0	0	FS	PS		0	0	0	0	0	0	0	0
all other addresses reserved for future expansion																									

Figure 10. Serial Interface Data Format

The first eight bits are the appropriate address for the instruction set and the remaining 16 bits are the instructions. The data is 24 bits long (3 bytes). Byte 1 is the address with A[7] being the MSB and A[0] being the LSB. Byte 2 and 3 program the IC with synthesizer information and PS (polarity select bit) information. D[15] is the MSB and D[8] the LSB. The PS bit selects which edge of the reference is used for frequency comparison. Improved spurious and phase noise is achieved by selected the edge with the fastest rise or fall time. If PS = 1, the rising edge is used as the reference. If PS = 0, the falling edge is used.

The filter select (FS) bit selects which receive filter path is enabled. If FS = 1, the *A* filter path is selected, if FS = 0 the *B* filter path is selected. This feature allows the user to control the receive signal bandwidth.

Each of the three lines in Figure 10 needs to be sent to the TRF1112 /TRF1212 to fully program the synthesizers, the FS bit, and the PS bit. Once the synthesizers and the FS/PS bits are fully programmed, the clock signal should be turned off to eliminate any clock-associated spurious signals

The UHF oscillator (LO2) frequency of oscillation is set by the following equation:

$$\text{Fout} = \text{REFIN} \times \left[8 \times (\text{N} + 3) - \text{S} - \frac{\text{F}}{18}\right]/8 \quad (1)$$

The S-band oscillator (LO1) frequency of oscillation is set by the following equation:

$$\text{Fout} = \text{REFIN} \times \left[8 \times (\text{N} + 3) - \text{S} - \frac{\text{F}}{18}\right] \quad (2)$$

where F has a range of 0 to 17. Both N and S have ranges that are limited more by the LO range than by their digital count.

Both synthesizers use a fractional architecture, which allows a high comparison frequency relative to the step size. The S-band PLL operates at a reference frequency of 18 MHz with a minimum phase accumulator frequency of 1 MHz. The UHF PLL operates at a 9-MHz reference with a minimum phase accumulator frequency of 0.5 MHz. The S-band PLL has a step size of 1 MHz and the UHF PLL has a step size of 125 kHz, when using an 18-MHz reference frequency. Different reference frequencies yield different step sizes, many of which are non-integer. If a different reference frequency is chosen, the step size is linearly related to the step size for 18 MHz.

Step size = step $\text{size}_{18\text{MHz}}$ x [REF FREQ/18 MHz]

In addition to normal reference spurious signals, fractional synthesizers have fractional spurs. The fractional spurs occur at an offset from the LO signal that is dependent on the difference between the LO frequency and integer multiples of the reference frequency. The spur locations can be found by the following process: divide the LO frequency by the reference frequency, take the remainder (fraction to the right of the whole number) and multiply by the reference frequency. This frequency is the difference between the actual LO frequency and an integer multiple of reference frequency. Fractional spurs will occur at this frequency and the reference frequency minus this frequency.

An example will best explain the process: if LO1 is set to 2206 MHz and an 18-MHz reference frequency is used, then 2206/18 is 122.55556. The difference between the LO1 and 122 × 18 MHz is:

0.55556 x 18 MHz = 10 MHz

The fractional spurs will occur at this frequency offset (10 MHz) from LO1 and:

18 MHz–10 MHz or 8 MHz from LO1.

The fractional spurious level varies with the offset from the LO since these spurious signals are attenuated by the loop filter response. The larger the offset from the LO, the lower the spur level. In general, spurs at offsets greater than 3 or 4 MHz are below –75 dBc and are not a concern. The worst fractional spurs levels occur when they are located at 1 MHz offset from the LO1 frequency. (Note: the fractional spur is offset from the LO1 frequency by 1 MHz when the difference between the LO1 and an integer multiple of the reference frequency is 1 or 17 MHz.)

Although both synthesizers have fractional spurs, for most applications the spurious signals from the UHF (LO2) synthesizer can be ignored because these spurs are attenuated by frequency dividers that are placed after the LO2 generation. In some frequency plans it is possible to offset LO1 and LO2, in a complementary manner, to avoid worst-case fractional spurs (i.e., 1-MHz offsets) on LO1 synthesizer.

VCO Tuning Characteristics

The TRF1121 / TRF1221 internal VCOs have the following frequency vs tune voltage characteristics.

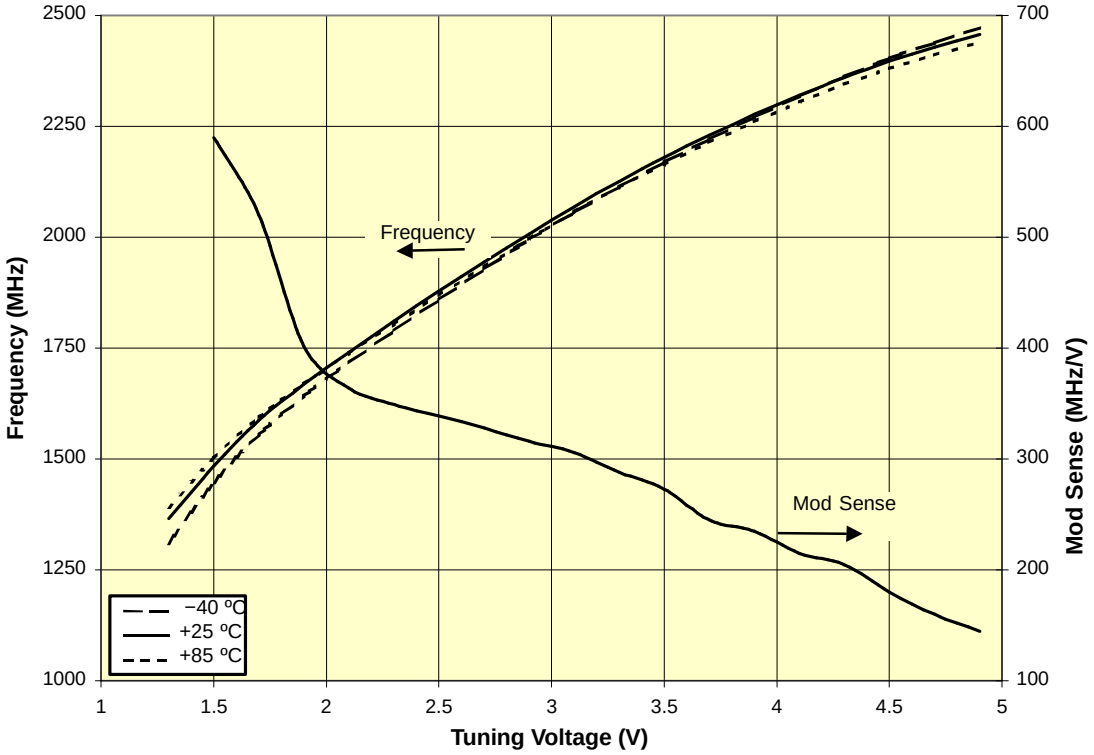


Figure 11. TRF1112 LO1 Frequency vs LO1TUN Voltage

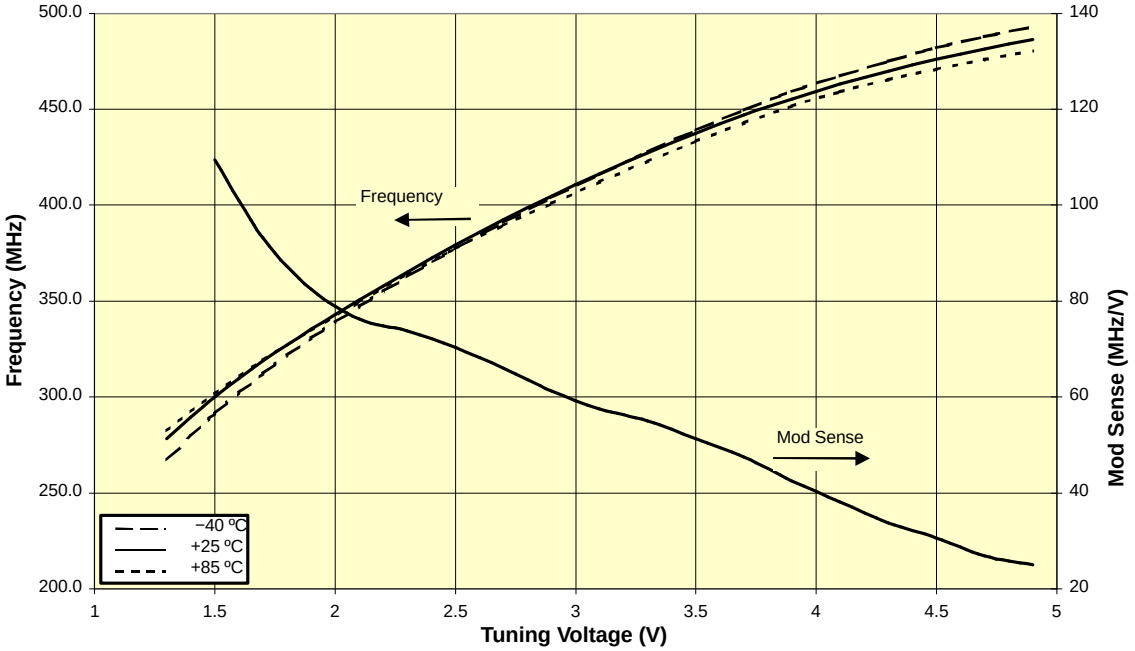


Figure 12. TRF1112 LO2 Frequency vs LO2TUN Voltage

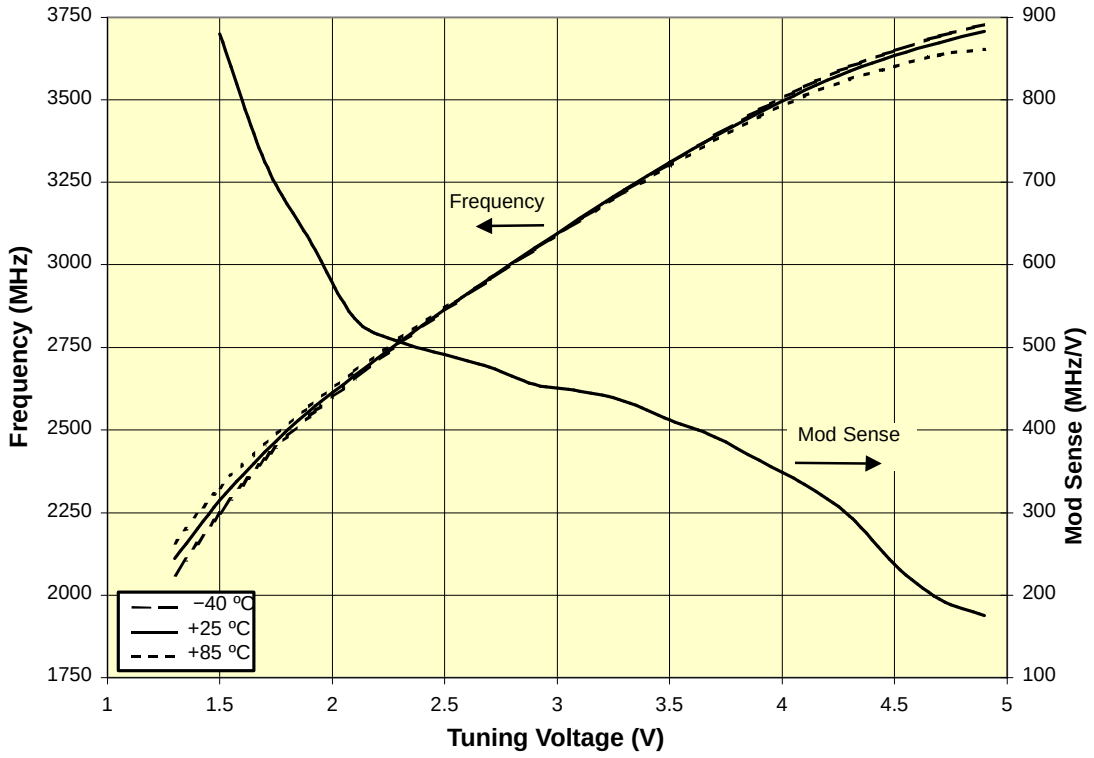


Figure 13. TRF1212 LO1 Frequency vs LO1TUN Voltage

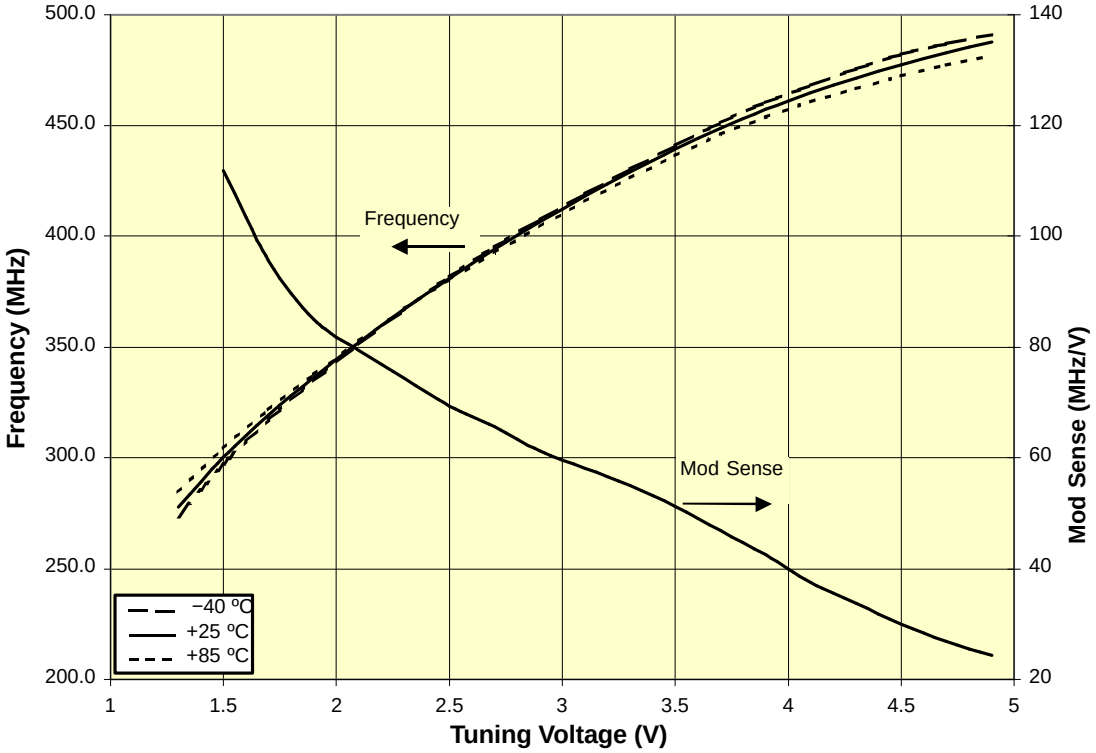


Figure 14. TRF1212 LO2 Frequency vs LO2TUN Voltage

Phase Noise

The TRF1112 / TRF1212 achieve superior phase noise performance with on-chip resonators and varactors. They are designed to meet the phase noise requirements of both single carrier and multi-carrier systems. Due to chip architecture, the phase noise and spurious performance of the LO2 (UHF) PLL is about 15 dB better than the LO1 (S-band) PLL. The typical phase noise of the TRF1112 and TRF1212 S-Band PLL (LO1) with the PLL locked is shown in Figure 15 and Figure 16, respectively. The phase noise of the TRF1212 S-Band PLL at the min and max range are shown in Figure 17 and Figure 18 respectively. These plots were taken at room temperature and typical voltage conditions.

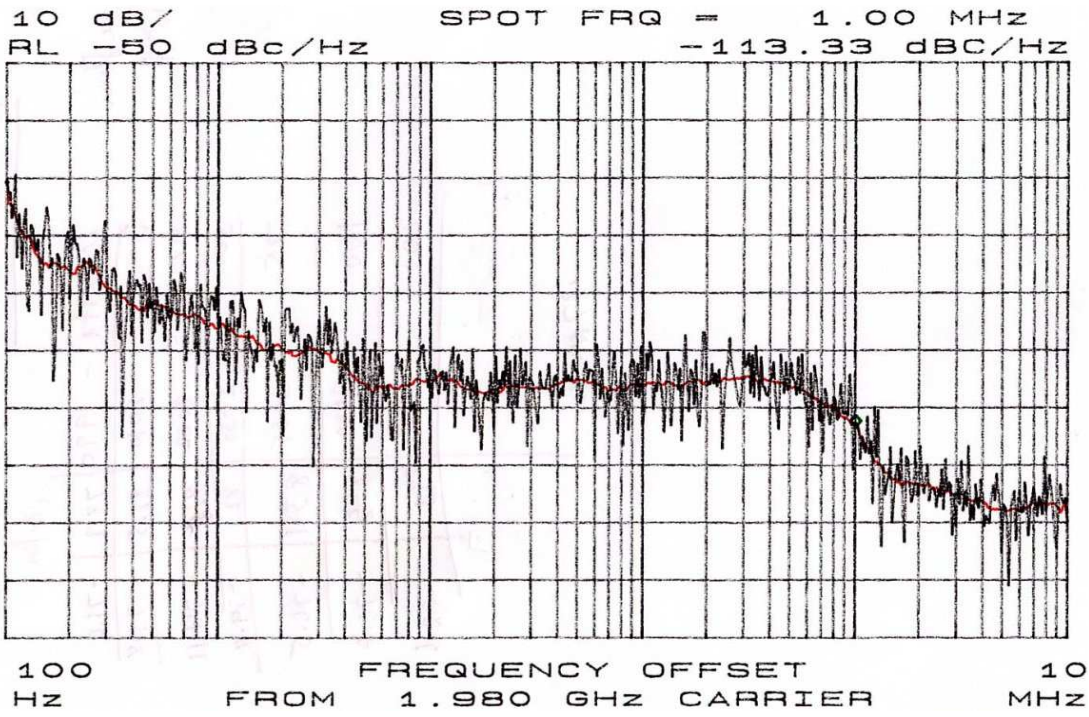


Figure 15. Phase Noise of TRF1112 Synthesizer #1 – Typical Performance is 0.4 RMS (100 Hz to 1 MHz)

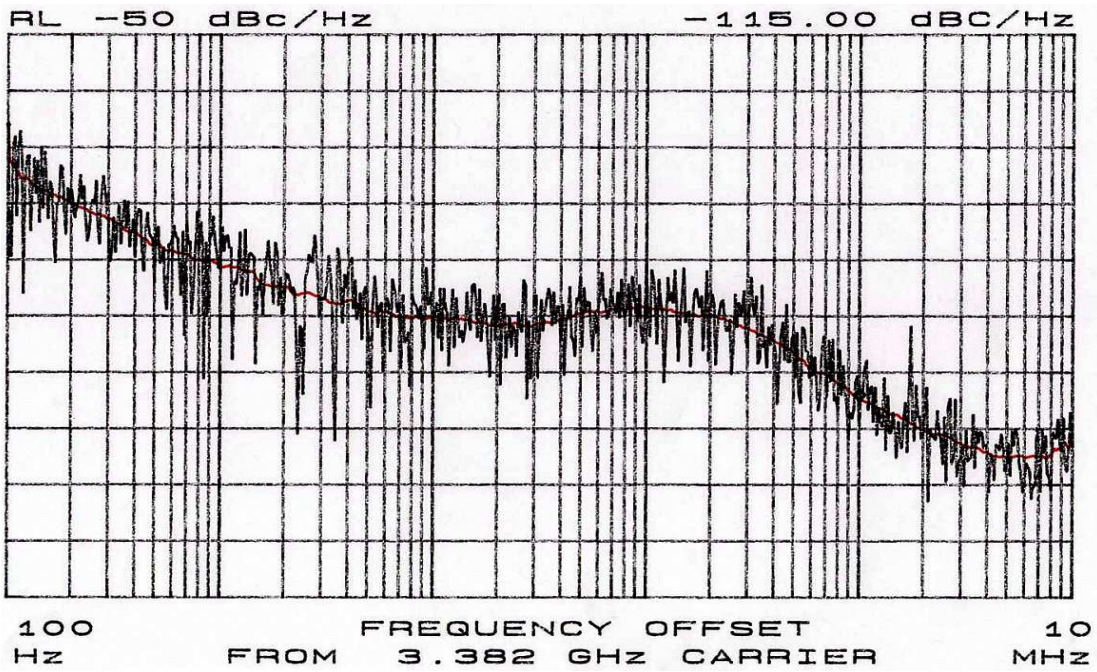


Figure 16. Phase Noise of the TRF1212 Synthesizer #1 – Typical Performance is 0.6 RMS (100 Hz to 1 MHz)

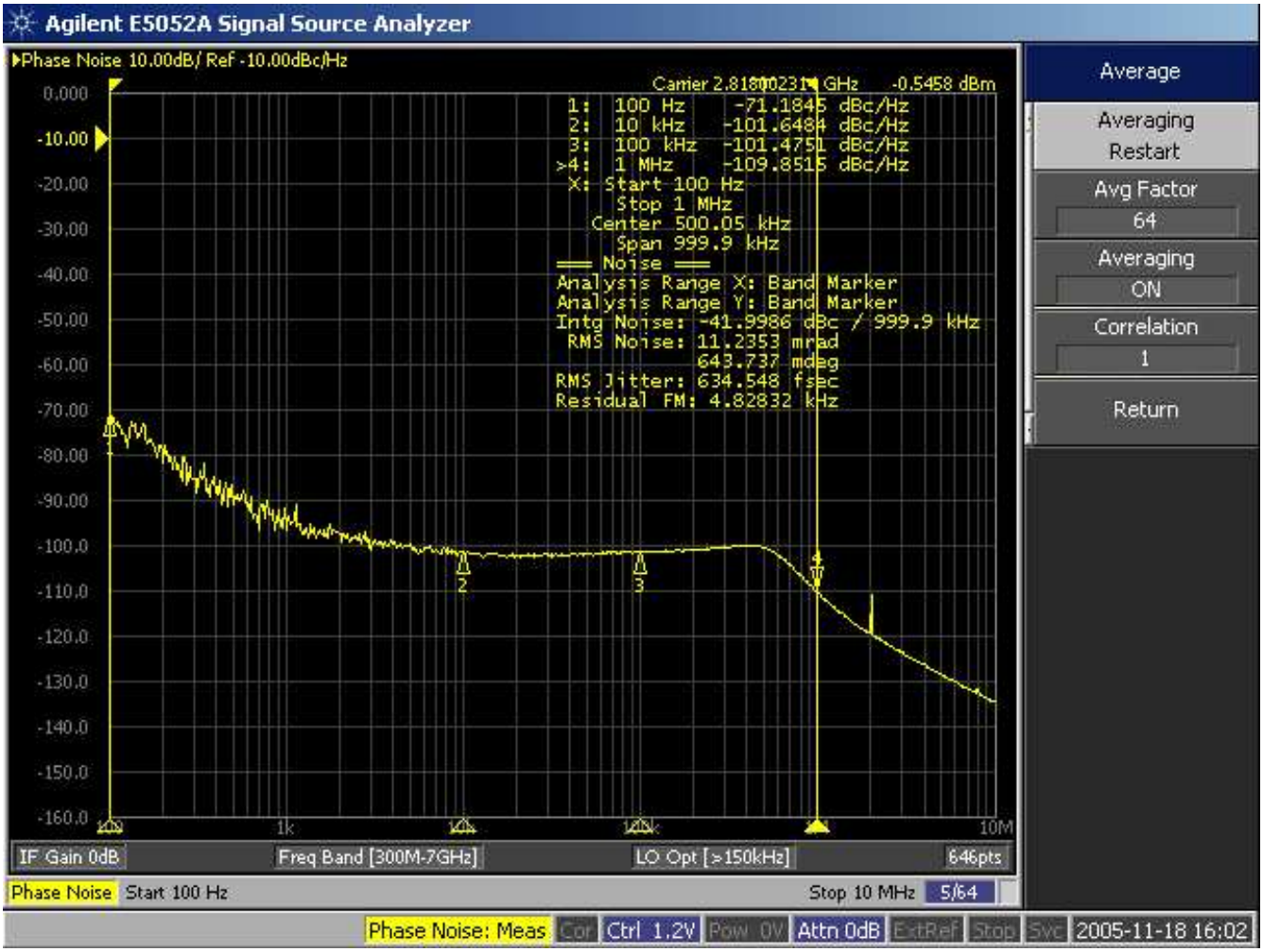


Figure 17. TRF1212 S-Band Synthesizer Phase Noise - 2818 MHz

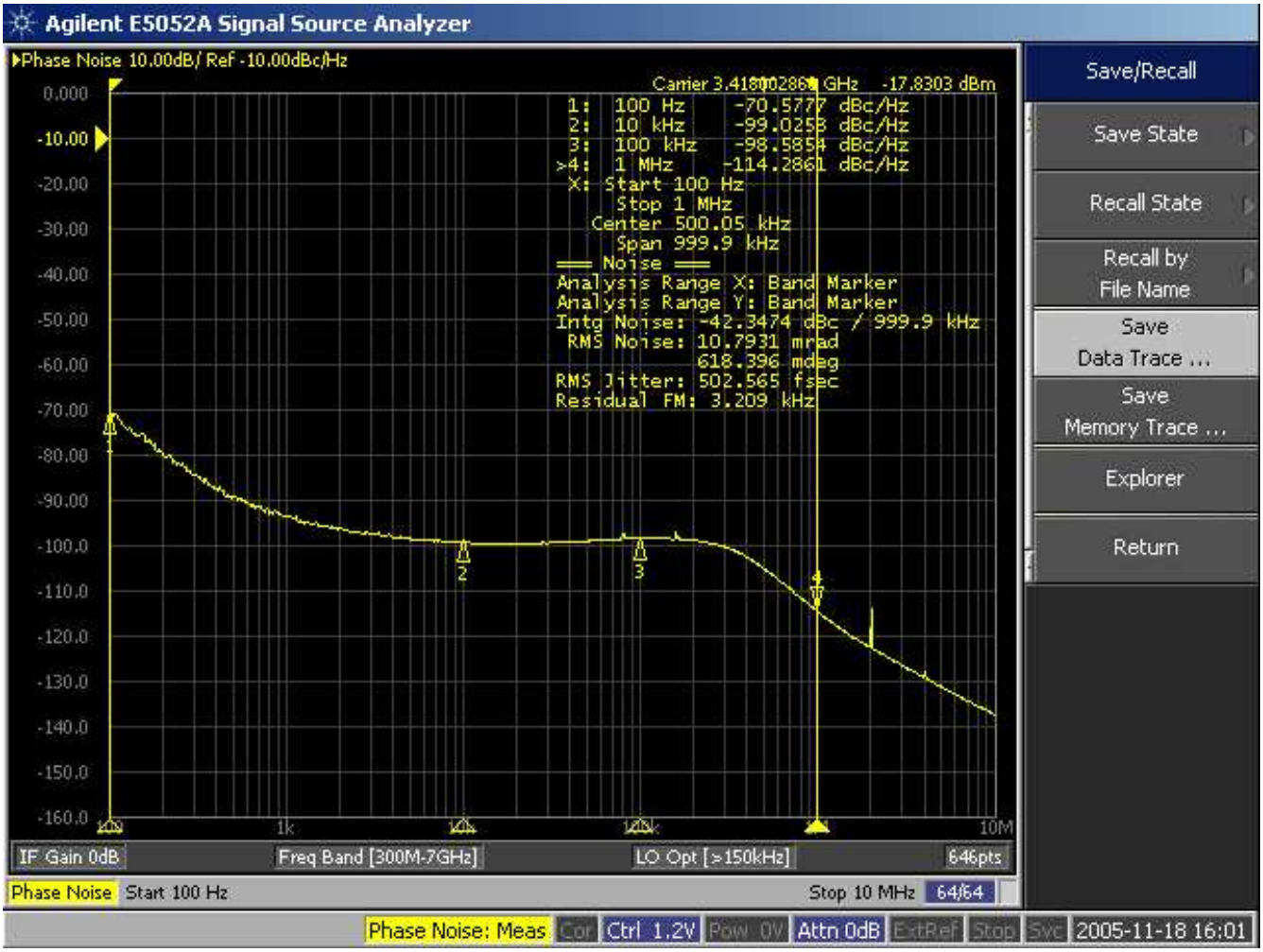


Figure 18. TRF1212 S-Band Synthesizer Phase Noise - 3418 MHz

For applications demanding tighter phase noise performance than that offered by Texas Instruments internal VCOs, a provision exists for connection of an external VCO. Texas Instruments integrated PLL locks the external VCO to the reference frequency and the chip provides an external tuning voltage that drives the VCO.

OUTPUT A/D INTERFACE

The output of the baseband amplifier is designed to directly drive typical A/D inputs. The output IF2 buffer amplifiers are low impedance emitter followers as shown in Figure 19.

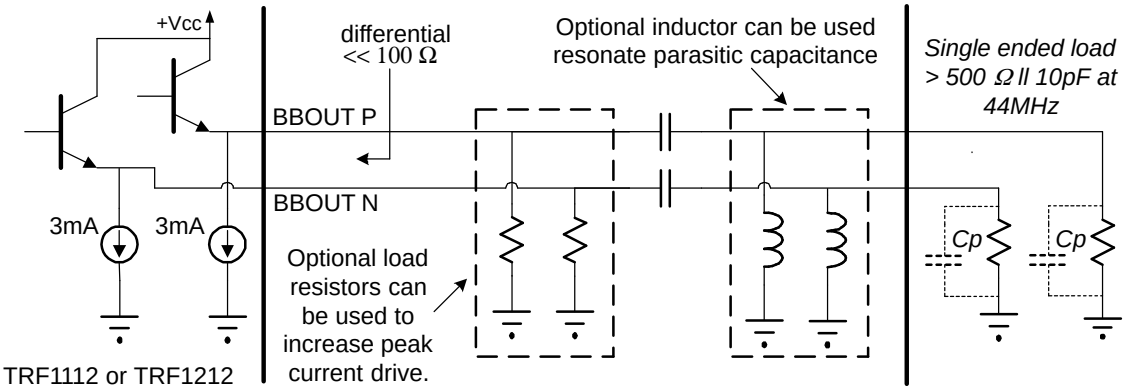


Figure 19. Output Interface for TRF1112 / TRF1212

The peak current drive of the output transistors is 3 mA. Assuming a 1.2-Vpp differential (0.6 V single ended) voltage swing, the minimum impedance the TRF1112 / TRF1212 drives without clipping is 0.6 V/3 mA = 200 Ω, single-ended. In practice the impedance must be higher to prevent distortion products from degrading BER of the receiver. This impedance must include the A/D input capacitance and any parasitic board capacitance. At 44 MHz, the TRF1112 / TRF1212 drives a differential impedance of 1000 Ω (single ended impedance of 500 Ω) with up to a 10-pF capacitive load (293-Ω single-ended impedance) and maintain 38-dBc imtermodulation products with 64 QAM modulation. Proper attention to layout and reduction of parasitic capacitance at this interface is critical to avoid linearity degradation. At higher IF frequencies parasitic capacitance is even more critical.

If parasitic capacitance is loading the output and degrading intermodulation performance there are two approaches to solve the problem. First a shunt inductor can be added to resonate the capacitance. The inductor value would be determined by: $L = 1/\omega^2 Cp$, where Cp is the parasitic capacitance and ω is 2π times the baseband receive IF frequency. Frequently this inductor can be part of the bias network for the ADC.

Second, the peak output current drive can be increased by adding a shunt resistor across the output of each baseband output. This resistor will essentially increase the quiescent current through the output transistor thus allowing a higher peak output current. The maximum **increase** in quiescent current is 3 mA resulting in a maximum allowable peak current of 6 mA. If load resistors are added, their resistance must be included to calculate total load impedance for the TRF1112 / TRF1212.

APPLICATION INFORMATION

A typical application schematic is shown in Figure 20 and a mechanical drawing of the package outline (LPCC Quad 7 mm × 7 mm, 48-pin) is shown in Figure 21.

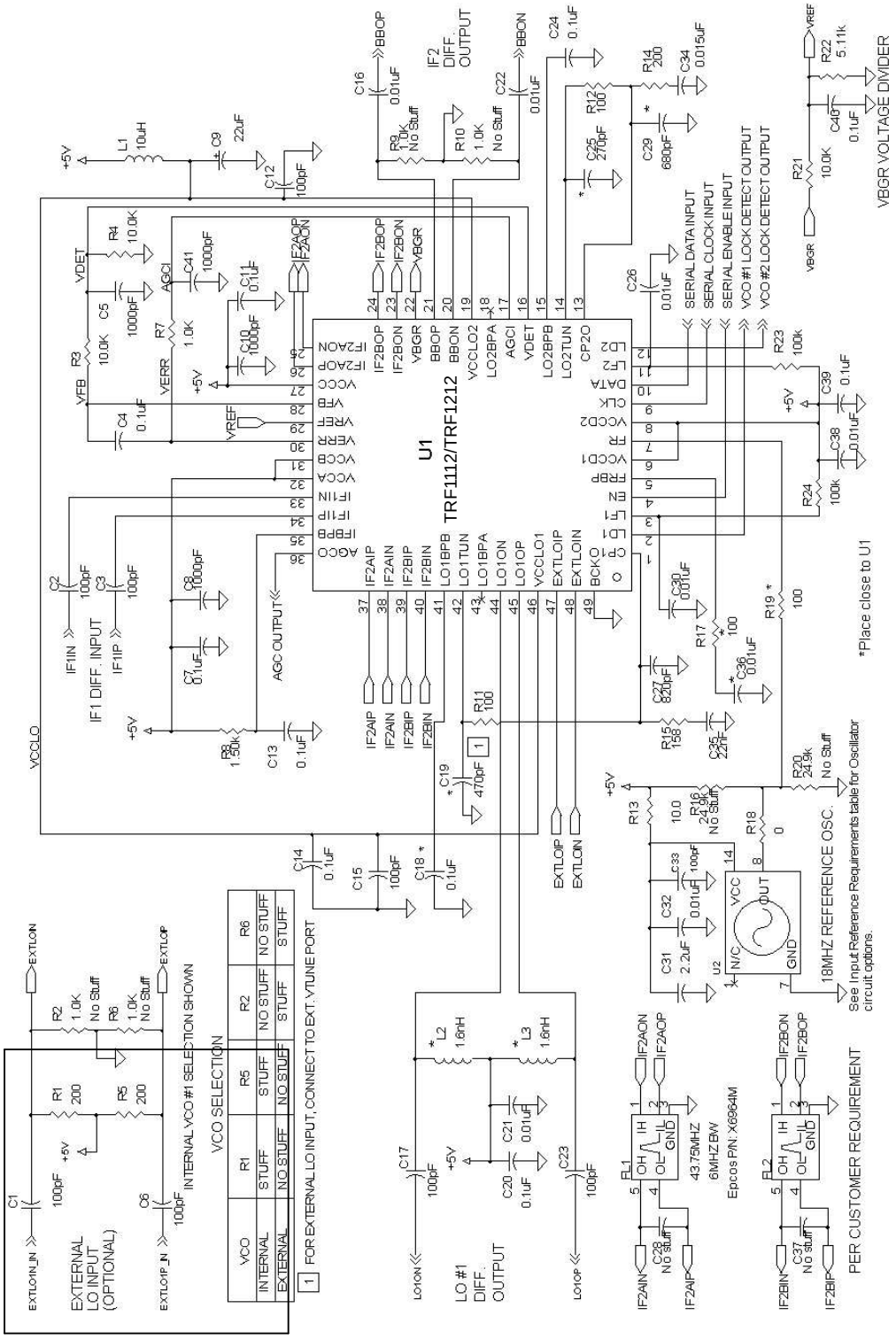
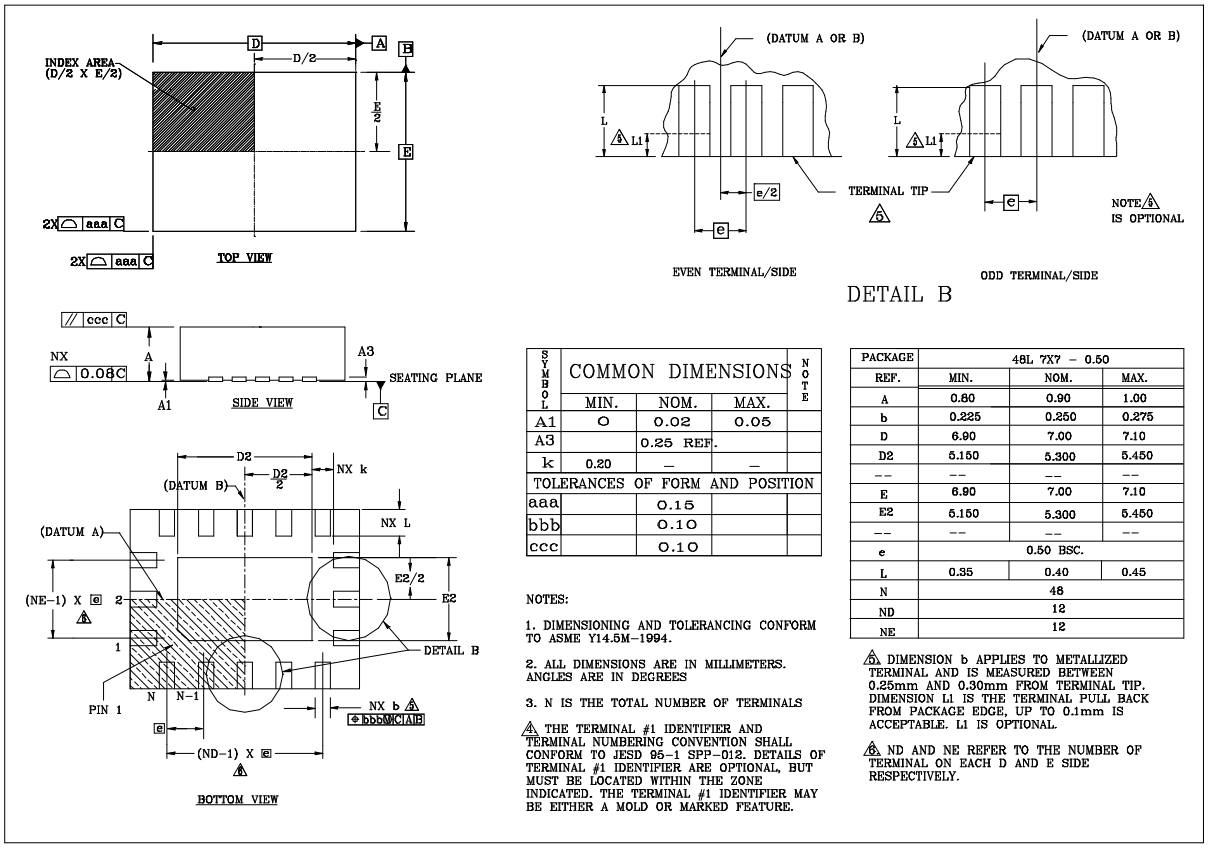


Figure 20. Recommended TRF1112/TRF1212 Application Schematic

APPLICATION INFORMATION (continued)



SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A1	0	0.02	0.05	
A3		0.25 REF.		
k	0.20	–	–	
TOLERANCES OF FORM AND POSITION				
aaa		0.15		
bbb		0.10		
ccc		0.10		

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES
3. N IS THE TOTAL NUMBER OF TERMINALS

4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

PACKAGE	48L 7X7 – 0.50		
REF.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
b	0.225	0.250	0.275
D	6.90	7.00	7.10
D2	5.150	5.300	5.450
--	--	--	--
E	6.90	7.00	7.10
E2	5.150	5.300	5.450
--	--	--	--
e	0.50 BSC.		
L	0.35	0.40	0.45
N	48		
ND	12		
NE	12		

5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 IS THE TERMINAL PULL BACK FROM PACKAGE EDGE, UP TO 0.1mm IS ACCEPTABLE. L1 IS OPTIONAL.

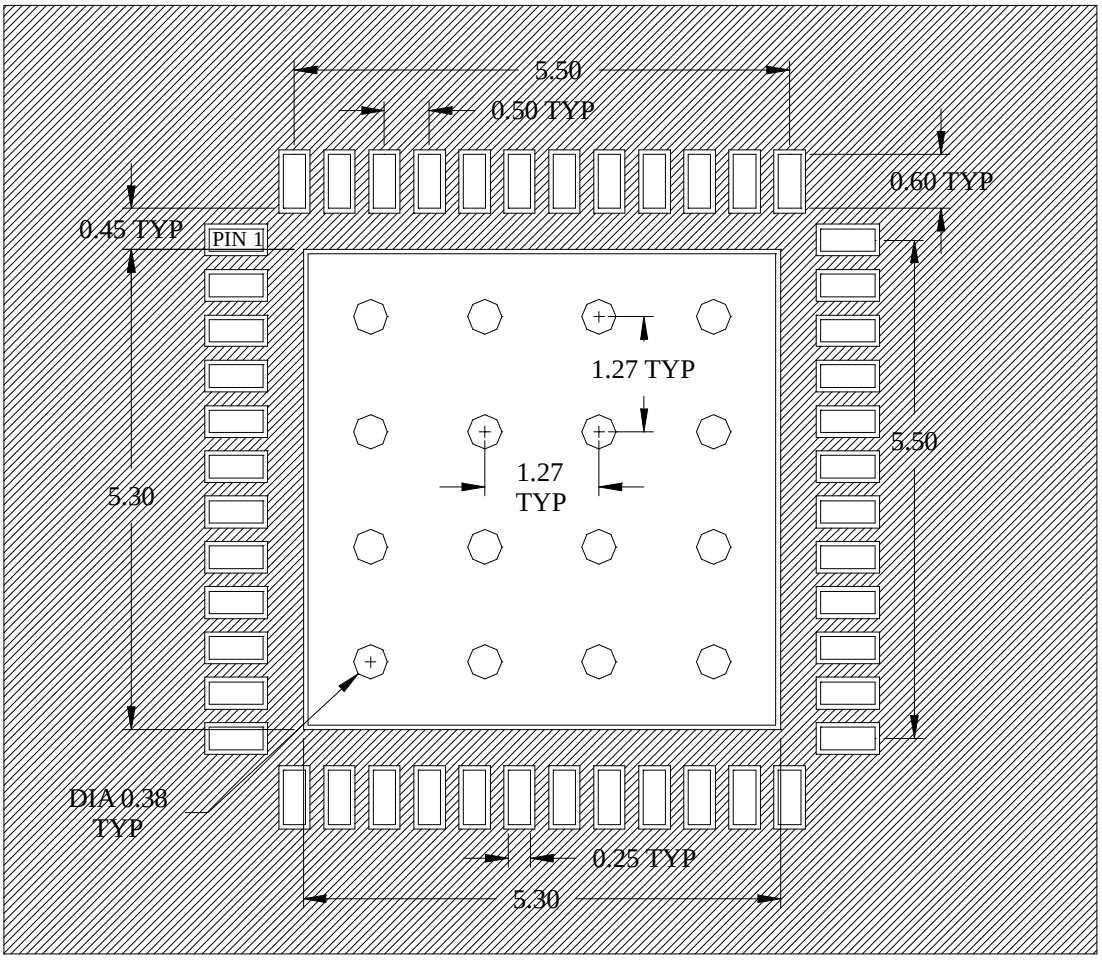
6. ND AND NE REFER TO THE NUMBER OF TERMINAL ON EACH D AND E SIDE RESPECTIVELY.

Figure 21. Package Drawing

The recommended PCB Layout mask is shown in Figure 22, along with recommendations on the board material (see Table 2) and construction (see Figure 23).

Table 2. PCB Recommendations

Board Material	FR4
Board Material Core Thickness	10 mil
Copper Thickness (starting)	1 oz
Prepreg Thickness	8 mil
Recommended Number of Layers	4
Via Plating Thickness	½ oz
Final Plate	White immersion tin
Final Board Thickness	33–37 mil

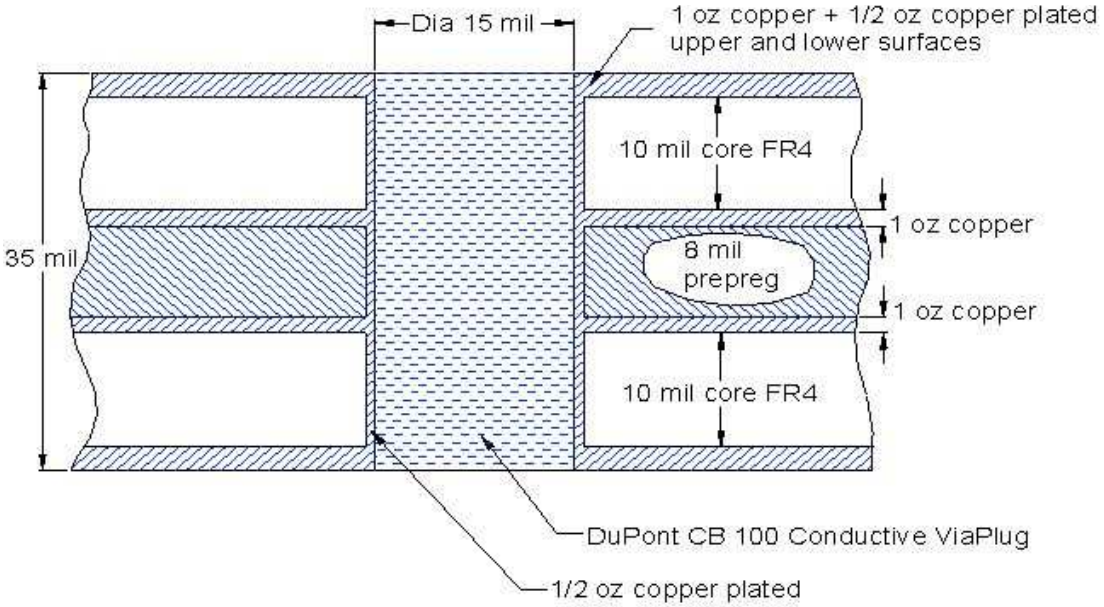


SOLDER MASK: NO SOLDERMASK UNDER CHIP, ON LEAD PADS OR ON GROUND CONNECTIONS.

16 VIA HOLES, EACH 0.38 mm.

DIMENSIONS in mm

Figure 22. Recommended Pad Layout

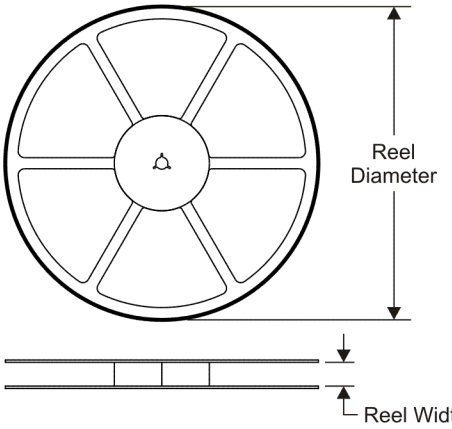


Note 1. Top and bottom surface finish: copper flash with 50-70 µin white tin immersion

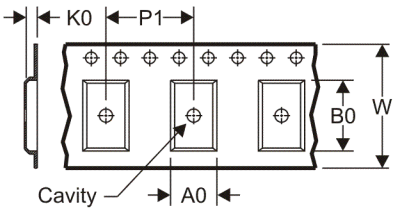
Figure 23. PCB Via Cross Section

TAPE AND REEL INFORMATION

REEL DIMENSIONS

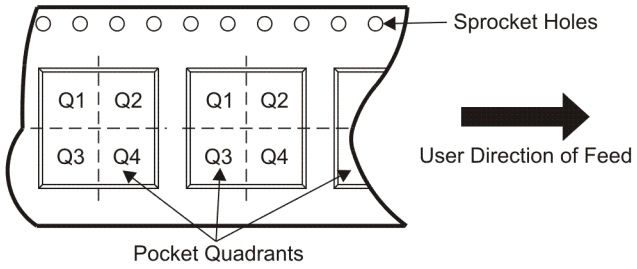


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

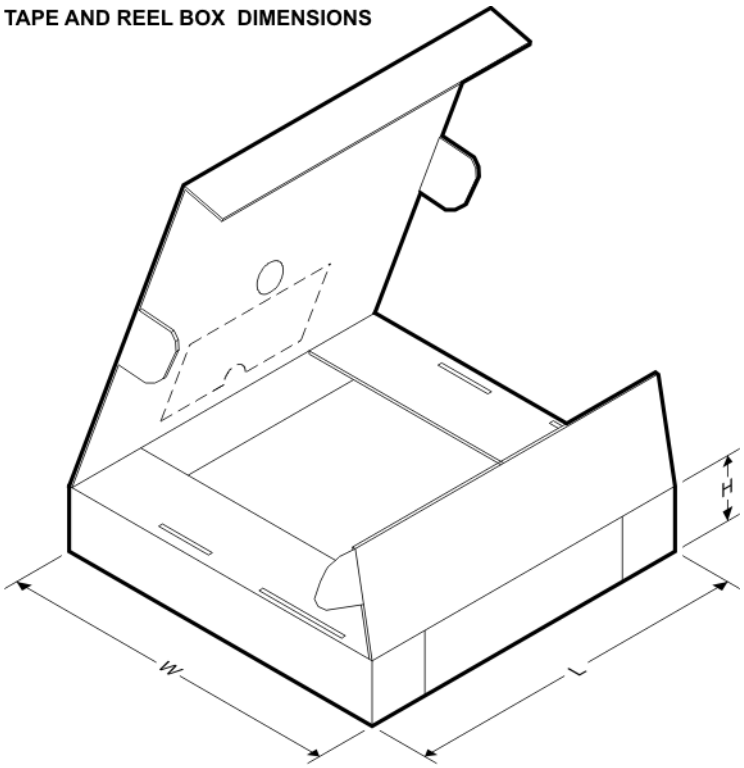
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF1112IRGZR	QFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TRF1112IRGZT	QFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TRF1212IRGZR	QFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TRF1212IRGZT	QFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

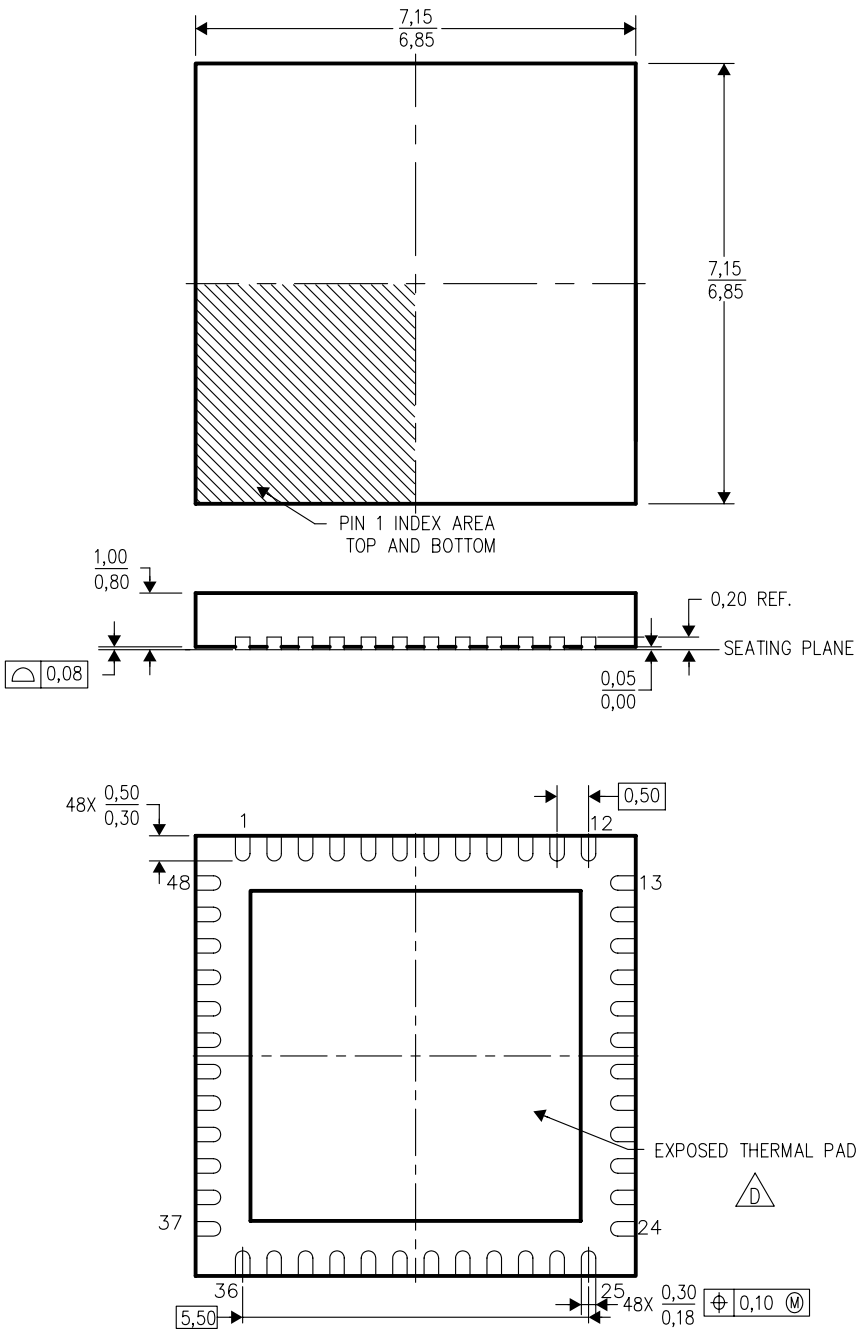
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF1112IRGZR	QFN	RGZ	48	2500	333.2	345.9	28.6
TRF1112IRGZT	QFN	RGZ	48	250	333.2	345.9	28.6
TRF1212IRGZR	QFN	RGZ	48	2500	333.2	345.9	28.6
TRF1212IRGZT	QFN	RGZ	48	250	333.2	345.9	28.6

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

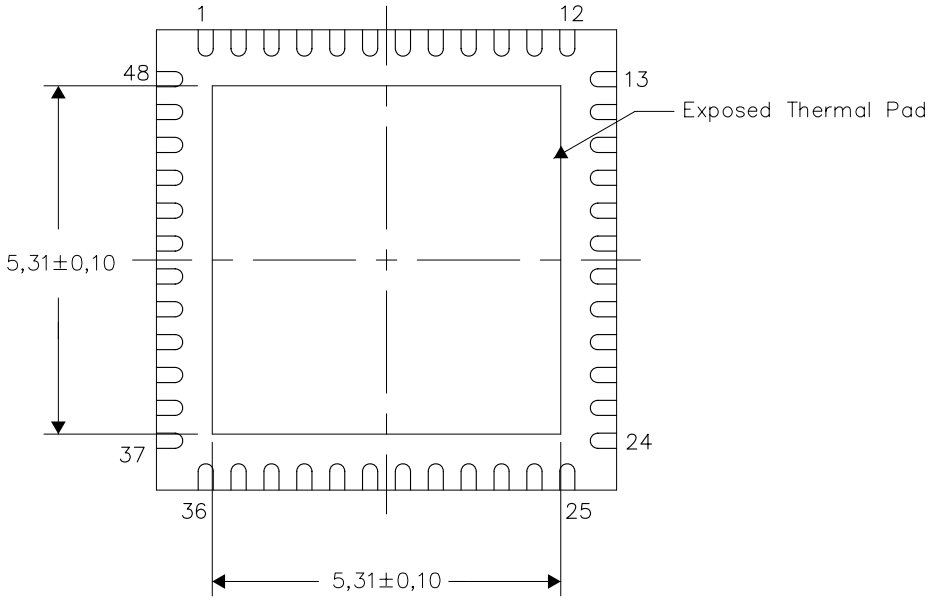
RGZ (S–PVQFN–N48)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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